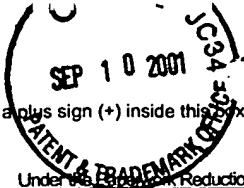


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Sheet 1 of 2

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Application Number	09/847,642
Filing Date	May 1, 2001
First Named Inventor	Mihai T. Lazarescu
Group Art Unit	Not Assigned 2124
Examiner Name	Not Assigned INGBERG
Attorney Docket Number	261/246

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
TI	AA	Prof. Dov Dori, <u>About OPCAT</u> , 2000, pages 1-2, http://iew3.technion.ac.il/~dori/opcat/about.htm1	
TF	AB	Prof. Dov Dori, <u>OPM Methodology</u> , 2000, pages 1-3, http://iew3.technion.ac.il/~dori/opcat/methodology.htm1	
TF	AC	Prof. Dov Dori, <u>OPCAT's Contents</u> , 2000, pages 1-5, http://iew3.technion.ac.il/~dori/opcat/contents.htm1	
TF	AD	Prof. Dov Dori, <u>Examples</u> , 2000, pages 1-3 http://iew3.technion.ac.il/~dori/opcat/example.htm1 (Fig. 1 and Fig. 2 did not display when website was viewed).	
TF	AE	Vojin Zivojnovic, Stefan Pees, Christian Schlaeger, Markus Willems, Rainer Schoenen and Heinrich Meyr, <u>DSP Processor/Compiler Co-Design A quantitative Approach</u> , ICSPAT, 1997, pages 761 - 765	
TF	AF	Guido Post, Vojin Zivojnovic and Sebastian Ritz, <u>Multiprocessor, Architecture Extension for the BlockDiagram-Oriented Design Tool Cossap/Descartes</u> , ICSPAT, 1995	
TF	AG	Stefan Pees, Vojin Zivojnovic, Andreas Hoffmann, Heinrich Meyr, <u>Retargetable Timed Instruction Set Simulation of Pipelined Processor Architectures</u> , ICSPAT, 1998	
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TF	AJ	Graham R. Hellestrand, <u>Designing System on a Chip Products Using Systems Engineering Tools</u> , 1999, pages 1-6, VaST Systems Technology Corporation	
TF	AK	Vojin Zivojnovic, Stefan Pees, Heinrich Meyr, <u>LISA - Machine Description Language and Generic Machine Model for HW/SW Co-Design</u> , October 1996, 1996 IEEE Workshop on VLSI Signal Processing, San Francisco	
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TF	AQ	Dr. Graham Hellestrand, <u>The Advent of the Virtual Processor Model</u> , E. E. Times, May 14, 1999, pages 1-7, VaST Systems Technology, Santa Clara, CA, USA	
TF	AR	Graham R. Hellestrand, <u>Systems Engineering: The Era of the Virtual Processor Model (VPM)</u> , April 14, 1999, pages 1-6, VaST Systems Technology, Santa Clara, CA, USA	
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Group Art Unit	Not Assigned 2124
Examiner Name	Not Assigned IUGBERG
Attorney Docket Number	261/246

Sheet 2 of 2

TR	AT	Soner Önder, Rajiv Gupta, <u>Automatic Generation of Microarchitecture Simulators</u> , May 1998, IEEE International Conference on Computer Languages	
TF	AU	Joachim Fitzner, ChrisSchläger, Davorin Mista, Vojin Zivojnovic, <u>Implementing LISA Tools Based on a DSP Architecture Description</u> , ICSPAT 1999	
TF	AV	Lisa Guerra, Joachim Fitzner, Dipankar Talukdar, Chris Schlager, Bassam Tabbara, Vojin Zivojnovic, <u>Cycle and Phase Accurate DSP Modeling and Integration for HW/SW Co-Verification</u> DAC 1999	
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TX	AY	Vojin Zivojnovic, Chris Schlager, Joachim Fitzner, <u>System-Level Modeling of DSP and Embedded Processors</u> , ASILOMAR 1998	

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